REMARKS

Applicant respectfully requests reconsideration of the subject application as amended. In response to the office action mailed 8/3/04, Applicant is filing this amendment. Please amend claims 20 and 25. Accordingly, claims 20-25 are currently pending.

In the latest office action, the Examiner has rejected claims 20-23 and 25 under 35 U.S.C. §102(b) and claim 24 under 35 U.S.C. §103(a), citing Bechade (US Patent 5,789,966) for all of the rejections.

Applicant submits that the new claims recite language that clearly distinguish over Bechade in that the claimed embodiments of the invention recite a multiplexer which does not employ a buffer between the passgate circuits and the output logic gate. This direct coupling of the passgate nodes to the output logic gate is one feature that reduces internal gate delay.

Bechade discloses a distributed (in spatial separation) multiplexer in which buffered inverters 24 are used to optimize performance of the multiplexer of Figure 1 (Bechade at col. 4, lines 16-23). The inverters are used to buffer the output of the multiplexer to restore fast signal transition time (col. 4, lines 1-14). The claimed embodiments of the invention utilize direct coupling at the output (without an output buffer/inverter) to reduce gate delay. A buffer (inverter) is not employed, since the multiplexer need not necessarily be a distributed multiplexer (as in Bechade). Accordingly, Applicant submits that this feature is now clearly defined in claims 20 and 25 and that the elements of the amended claims distinguish over Bechade.

In response to the Examiner's comment about the phrase "wide bit-width input", Applicant has defined the bit width to be at least 4 bits for each of the passgate circuits.

Accordingly, Applicant respectfully requests the Examiner to withdraw the 35 U.S.C. §102(b) and 35 U.S.C. §103(a) rejections and allow amended claims 20-25.

If there are any fee shortages related to this response, please charge such fee shortages to Deposit Account No. 50-2126.

Respectfully submitted,

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Date: 11-3-04

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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

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